# Reliable, Low Cost Distributed Generator/Utility System Interconnect

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***GE Corporate Research & Development***
***GE Power Systems Energy Consulting***
***Puget Sound Energy***


**DOE Distributed Power Program**
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|---|---|
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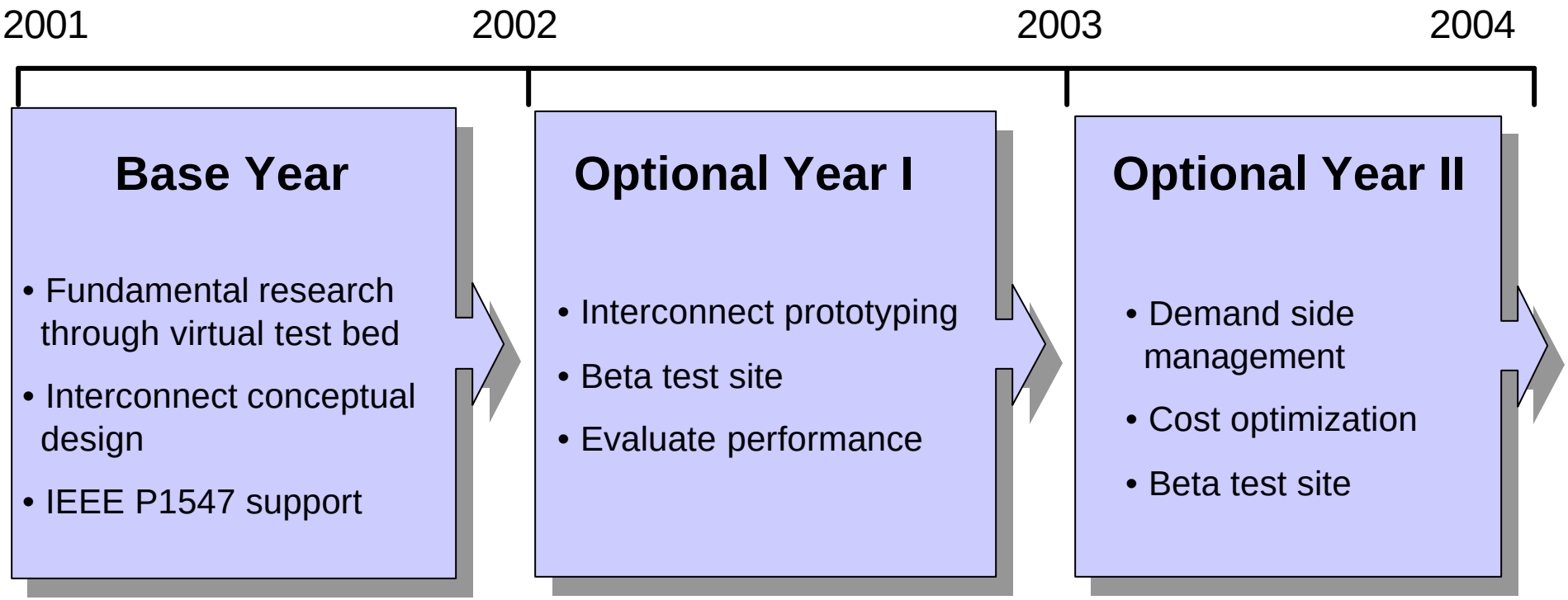
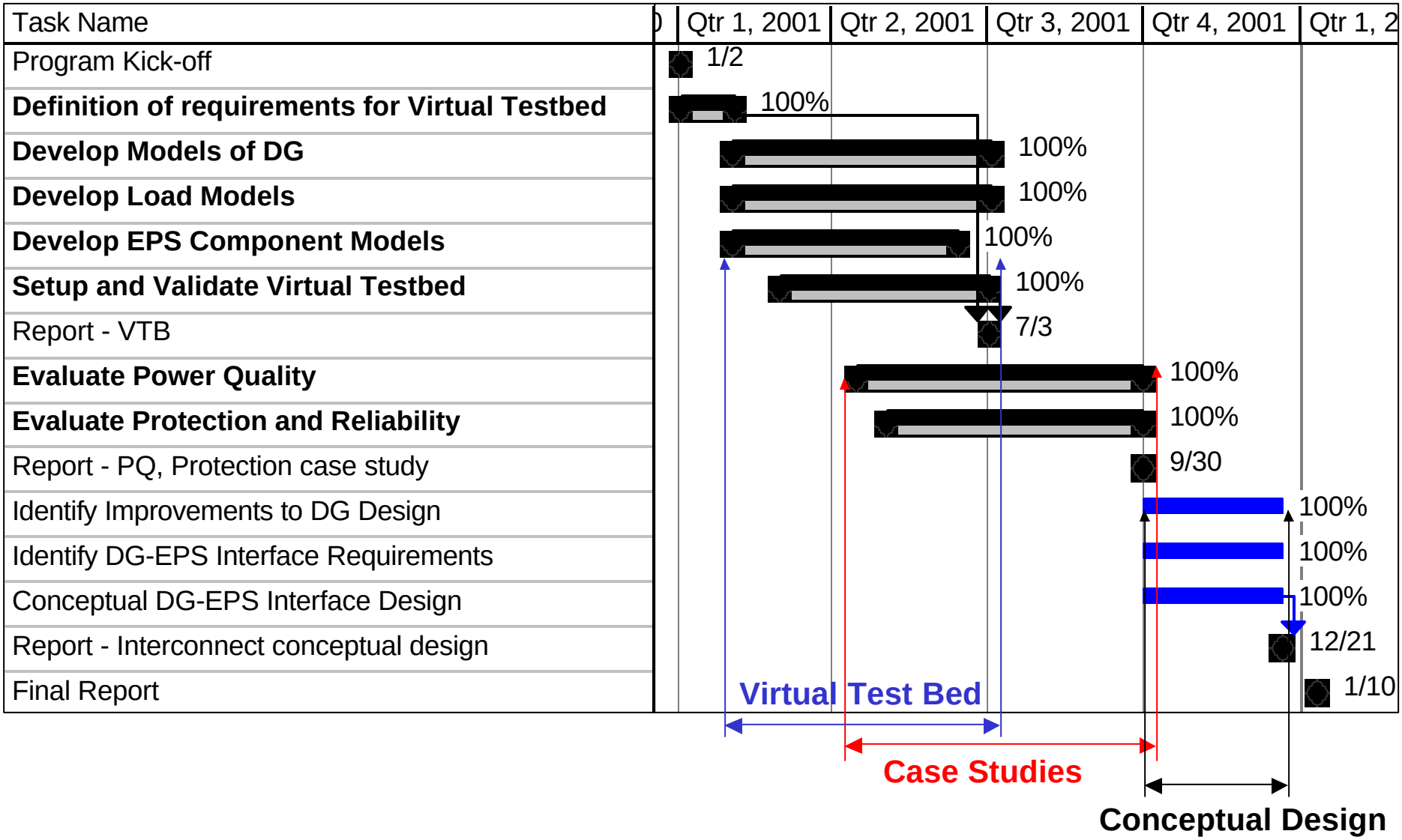
# Program Overview



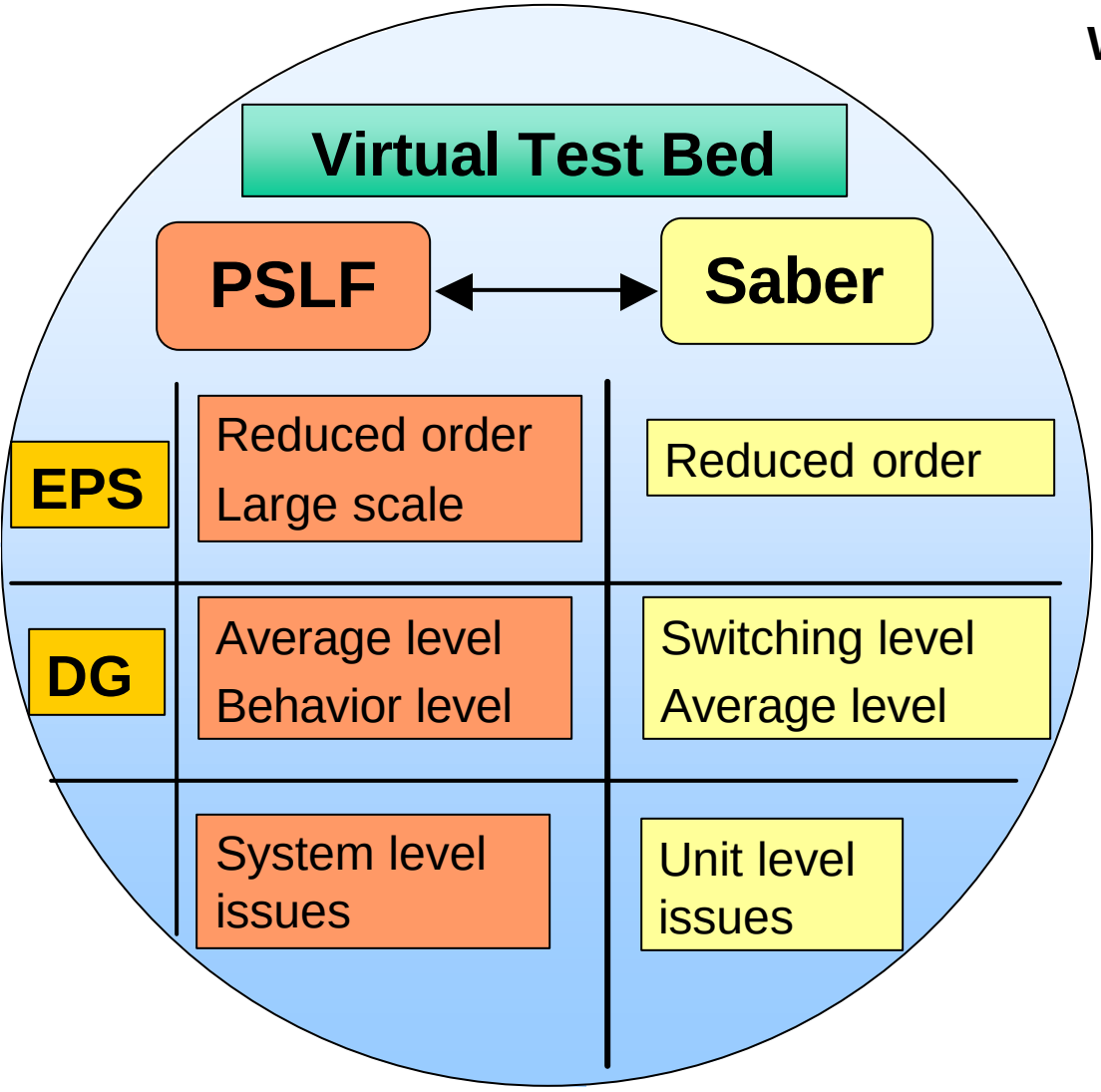

**Program Goals:**

- Explore DG/EPS system integration issues
- Develop DG/EPS interconnect solutions to allow reliable system operation, to overcome interconnection barriers, and to maximize DG benefits.

# Base Year Milestones and Deliverables



# Virtual Test Bed - Structure




**Why Saber and PSLF?**

- Saber - powerful system modeling tools for mixed technologies
  - Detailed component modeling
  - Modeled by differential equations

$$V = R \cdot I + L \cdot {dI}/{dt} + C \cdot \int I \cdot dt$$

  - High bandwidth
  - Handle small-scale systems
- PSLF - industry standard modeling tool for analyzing large system response
  - "Fundamental Frequency Program"
  - Modeled algebraically

$$\tilde{V} = \tilde{I} \cdot (R + j \cdot (X_L - X_C)$$

  - < 5 Hz modulation bandwidth
  - Electromechanical oscillations and some controls modeled dynamically
  - Handles very large systems

# Case Studies

Objectives:

- To evaluate DG impact on EPS power quality, protection and stability
- To identify fundamental requirements for defining interconnection system
- To quantify issues now confronting P1547, for example, how realistic are the impact, what penetration is required.

## Power Quality

- **Voltage Regulation**
- Flicker
- Unbalanced grid
- Harmonics
- DC current injection
- Grounding

## Protection and Stability

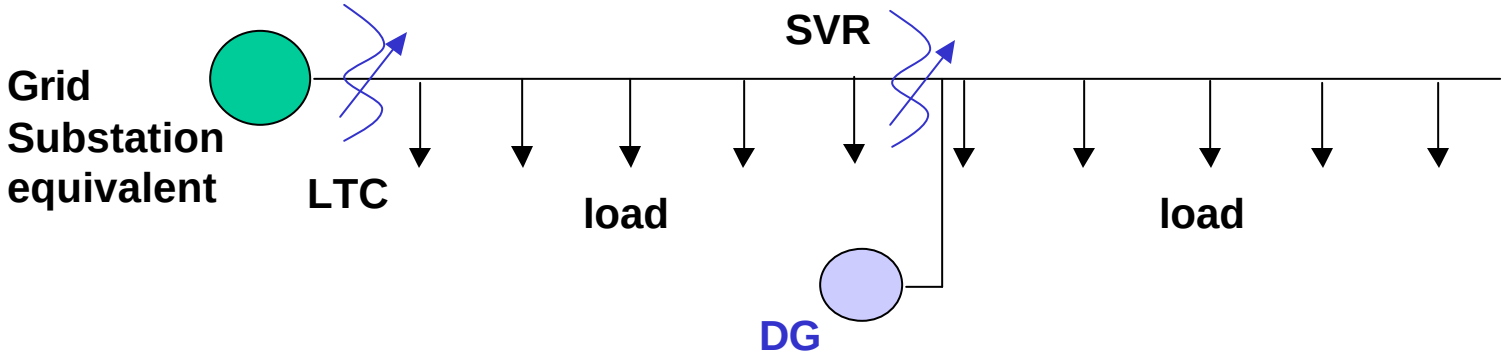
- Capacitor switching
- Fault analysis
- **Anti-islanding protection**
- Reclosing
- Stability
  - Local system stability
  - **Bulk system stability**
  - Microgrid stability

# Case Study - Voltage Regulation

**Objectives:**

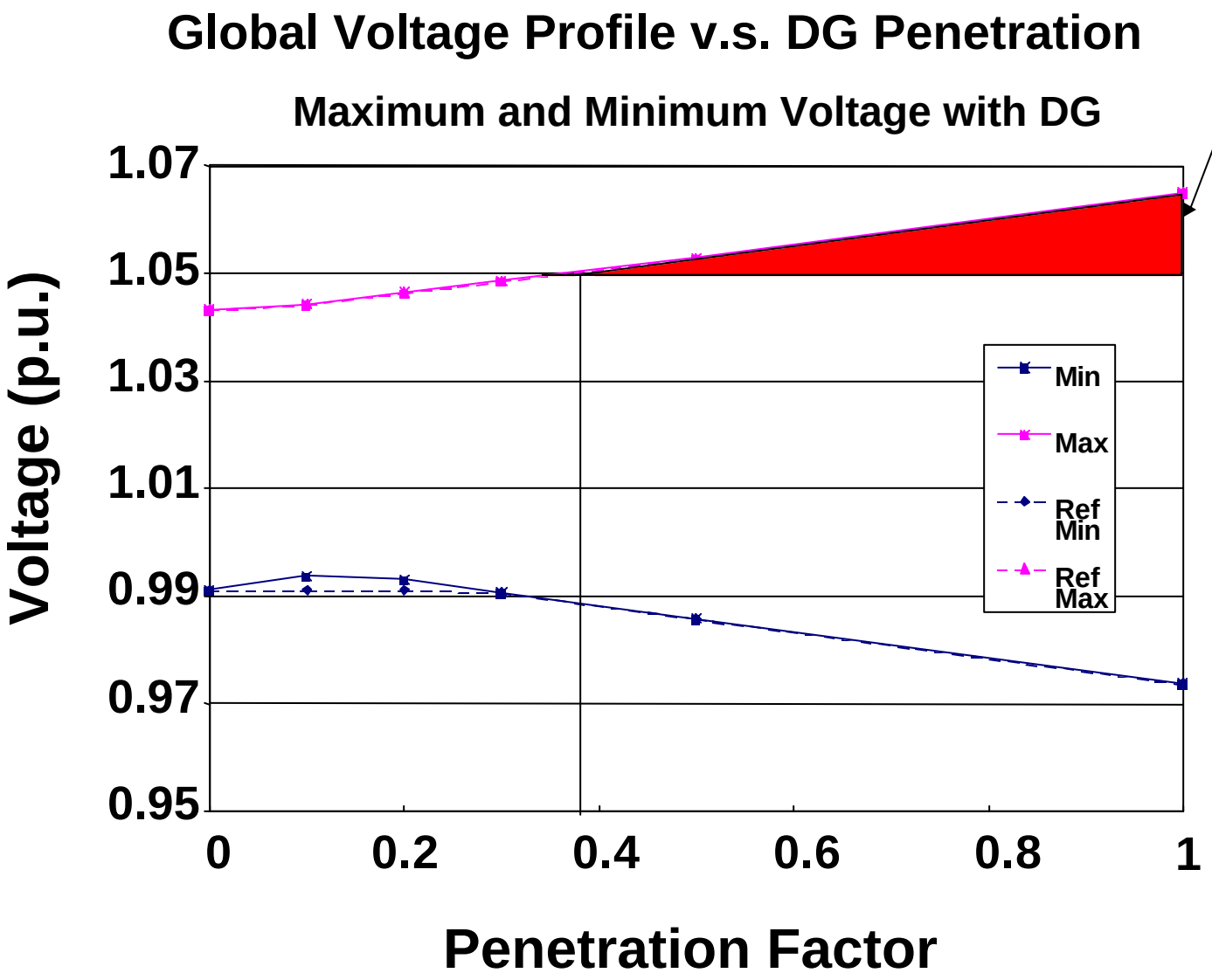
- **Study DG impact on feeder voltage profile**
- **Study DG interaction with LTC and SVR**

## Case 1: Generic Radial Feeder Models and Cases for Voltage Regulation Study



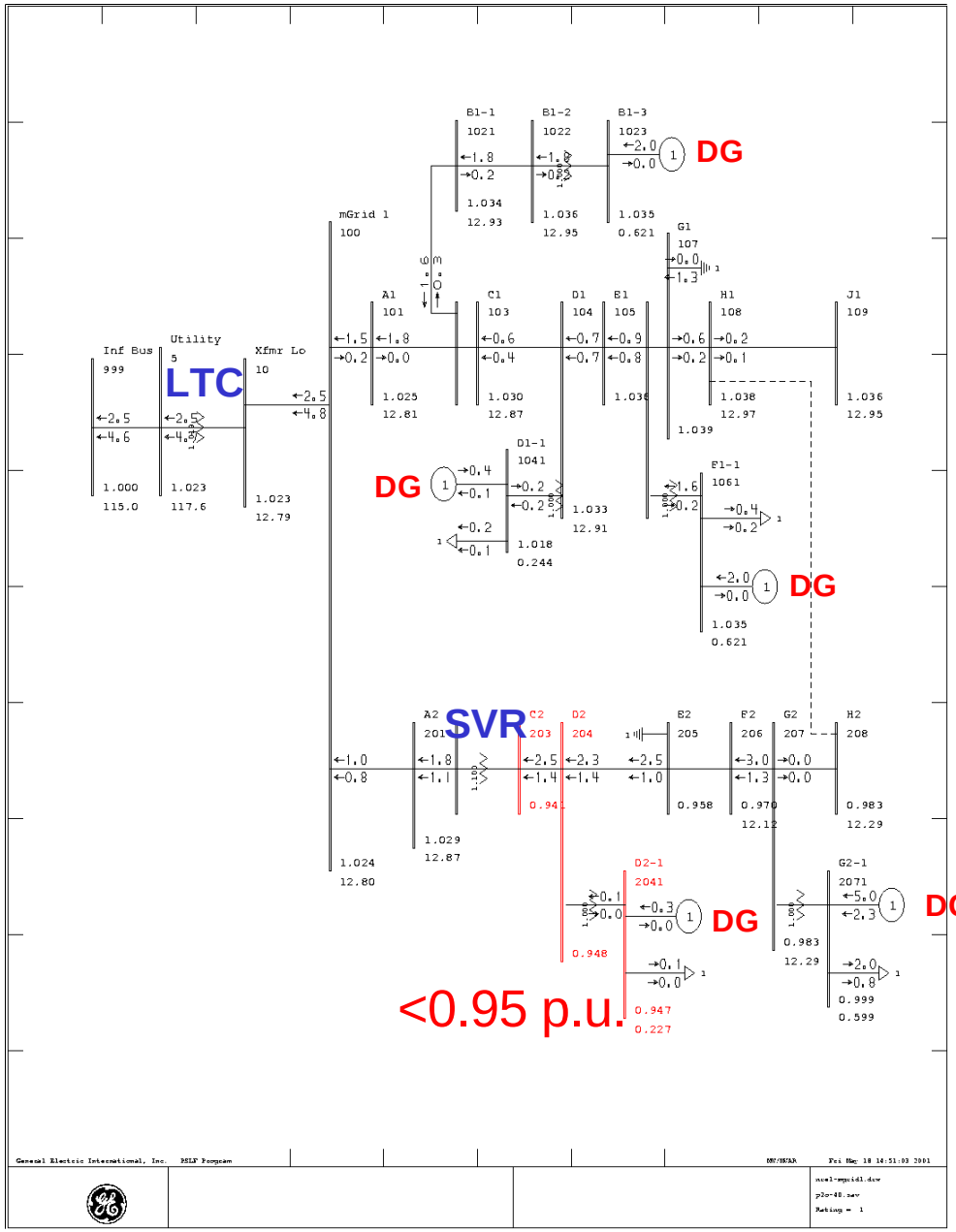

| Base Design | Design Variation | Substation LTC Control | | | | CAPACITOR BANKS[1] kVAr Rating* | SVR Control | | | | DG Voltage Regulation[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Voltage Setpoint | Load Drop Compensation Settings | | | | Voltage Setpoint | Load Drop Compensation Settings | | | |
| | | | R (W) | X (W) | Voltage Limit | | | R (W) | X (W) | Voltage Limit | |
| Case 1: 4 mile Feeder | 1.1 | 1.05 | No LDC | | Fixed | 0 | -No SVR- | | | | Secondary |
| | 1.2 | 1.04 | 0.30 | 0.60 | 1.05 | 0 | No SVR | | | | Secondary |
| | 1.3 | 1.05 | 0.00 | 0.00 | 1.05 | Varied[2] | No SVR | | | | Secondary |
| Case 2: 8 mile Feeder | 2.1 | 1.01 | 0.75 | 1.50 | No limit | 900 | No SVR | | | | Secondary |
| | 2.2 | 1.02 | 0.60 | 1.10 | 1.05 | 1200 | No SVR | | | | Secondary |
| Case 3: 8 mile Feeder | 3.1 | 1.02 | 0.50 | 1.00 | No limit | 900 | 1.01 | 1.00 | 2.00 | No limit | Secondary |
| | 3.2 | 1.03 | 0.25 | 0.50 | 1.05 | 900 | 1.03 | 0.60 | 1.10 | 1.05 | Secondary |
| | 3.3 | 1.03 | 0.25 | 0.50 | 1.05 | 900 | 1.03 | 0.60 | 1.10 | 1.05 | Primary |

# Case Study - Voltage Regulation




DG can cause high voltages at light load for significant penetrations

# Case Study - Voltage Regulation

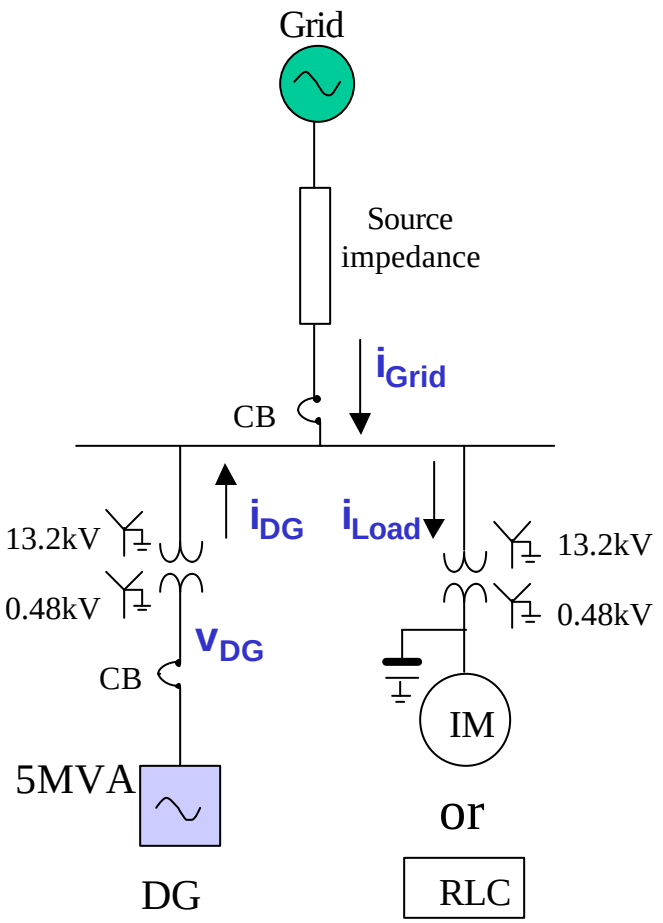


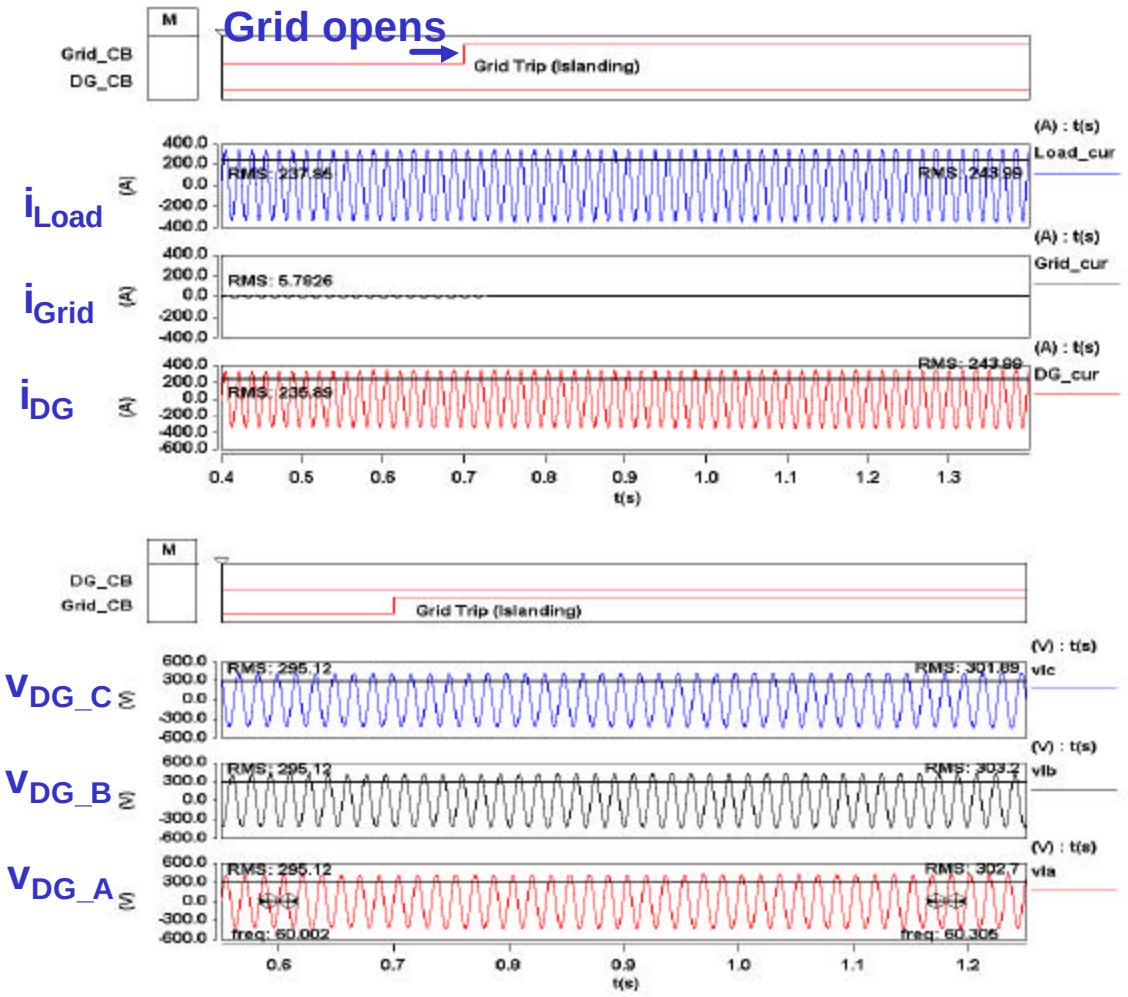

## Case 2:
## DG interaction with SVR

- SVR adjusts voltage set points based on locally measured real and reactive current flow.
- The presence of DG (5 DGs in this example) causes localized changes in flow patterns
- The interaction may cause unstable SVR regulation and result in out-of-range voltage (0.94 p.u.), as highlighted in the Figure.

# Case Study - Anti-Islanding

**Objective:**
**Study worst-case load using Sandia's scheme as an example.**



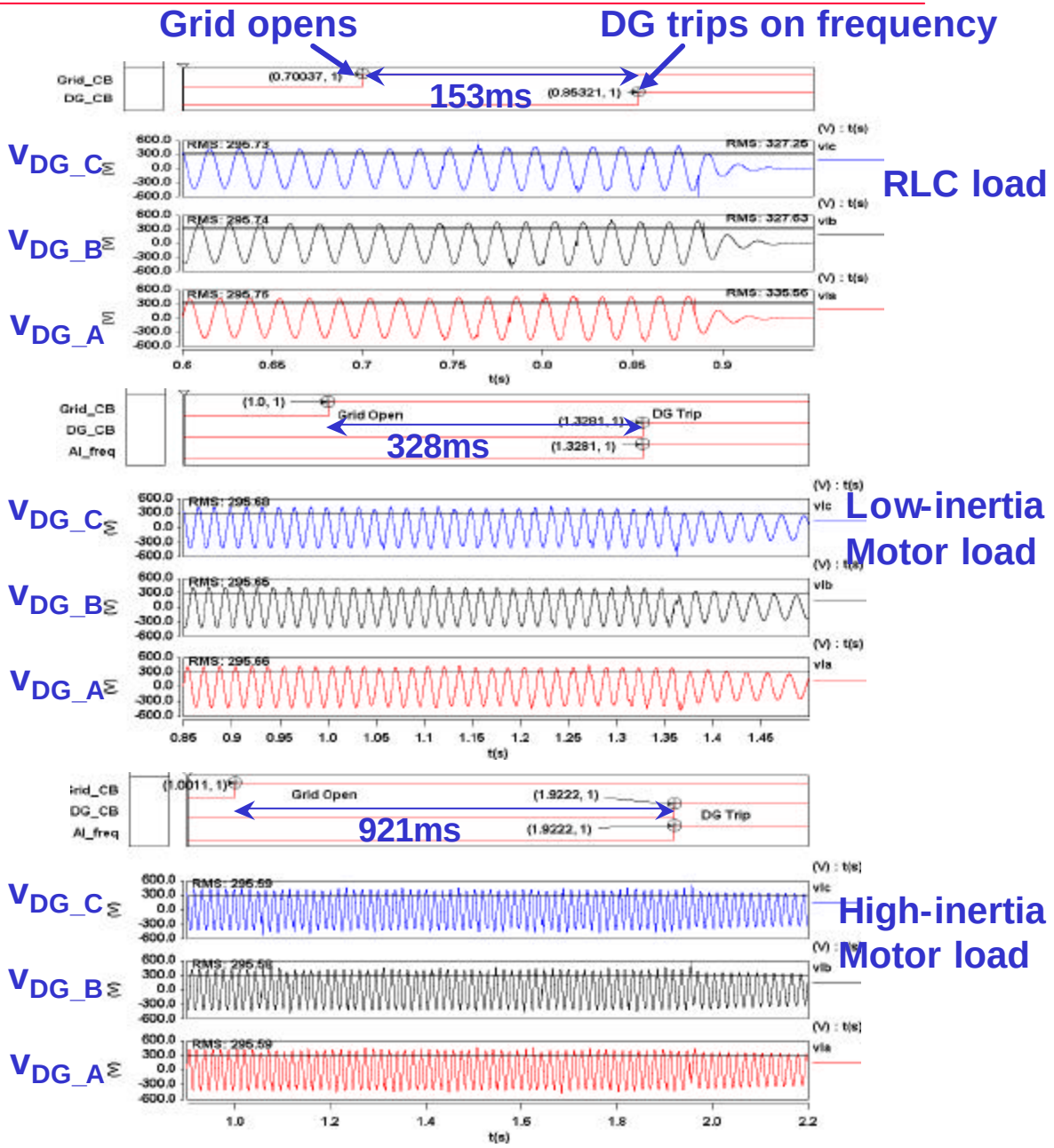




- Without active anti-islanding, it is highly possible that an island may be formed if DG and load are closely matched

# Case Study - Anti-Islanding

- Active anti-islanding can detect island condition with different loads.

- There is much longer run-on time for high-inertia motor load than RLC load and low-inertia motor load. Therefore, motor load is more challenging for anti-islanding detection.

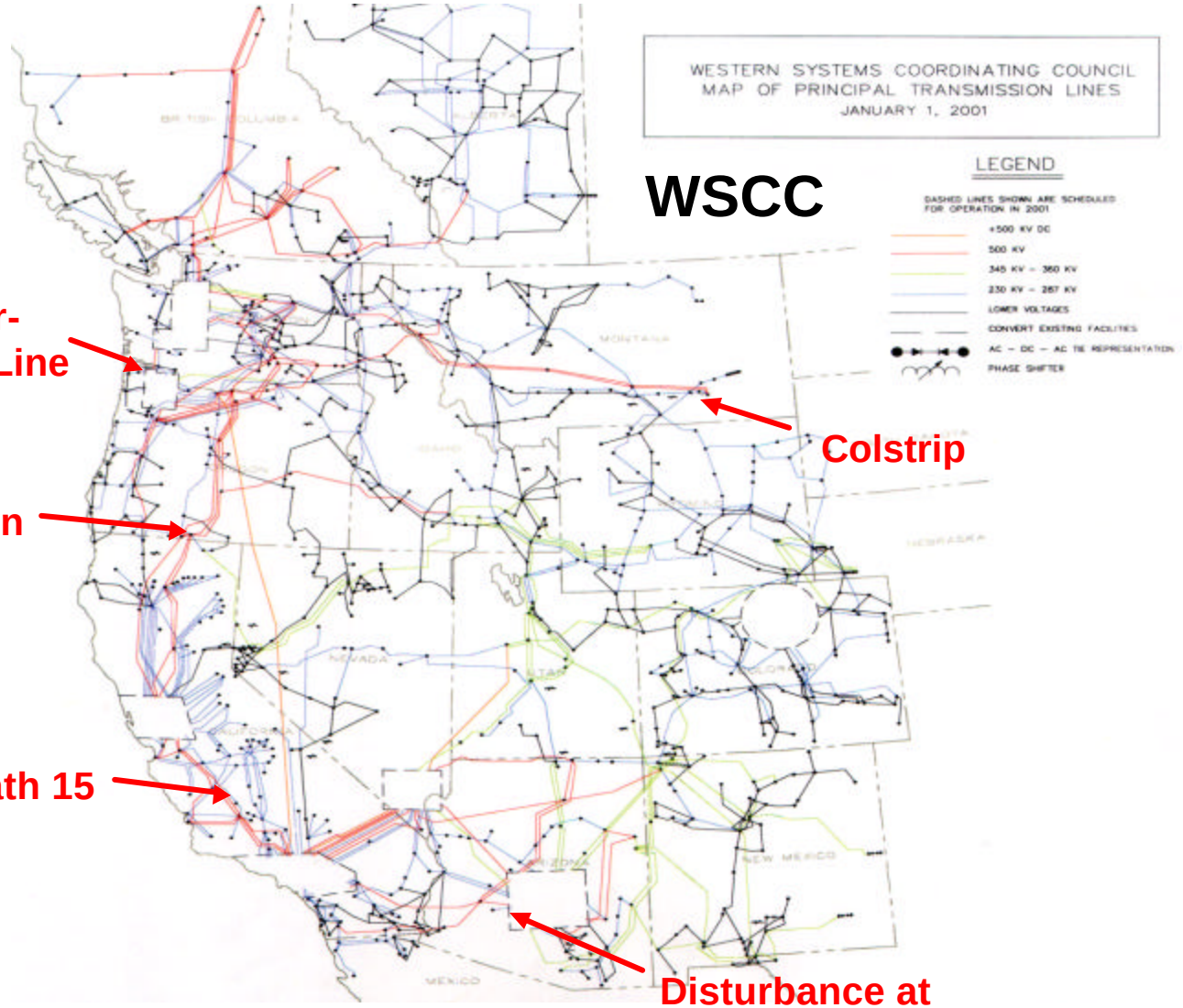


# A Look at Future with High DG Penetration

- What might DGs do to the dynamics of a distribution feeder?
- What might DGs do to the dynamic of an entire bulk power system?
  - *Will transient stability be affected?*
  - *Will damping be impacted?*
  - *Will voltage stability be affected?*

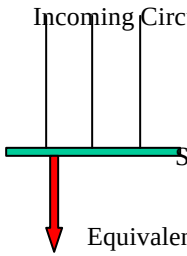
**Are there actions that the industry might take now, to make high penetration of DGs beneficial to the power system as a whole?**

# Case Study - DG Impact on Bulk Power System



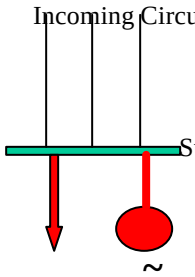

**>6000 DGs Modeled:**

**Base Case Load Bus Representation**



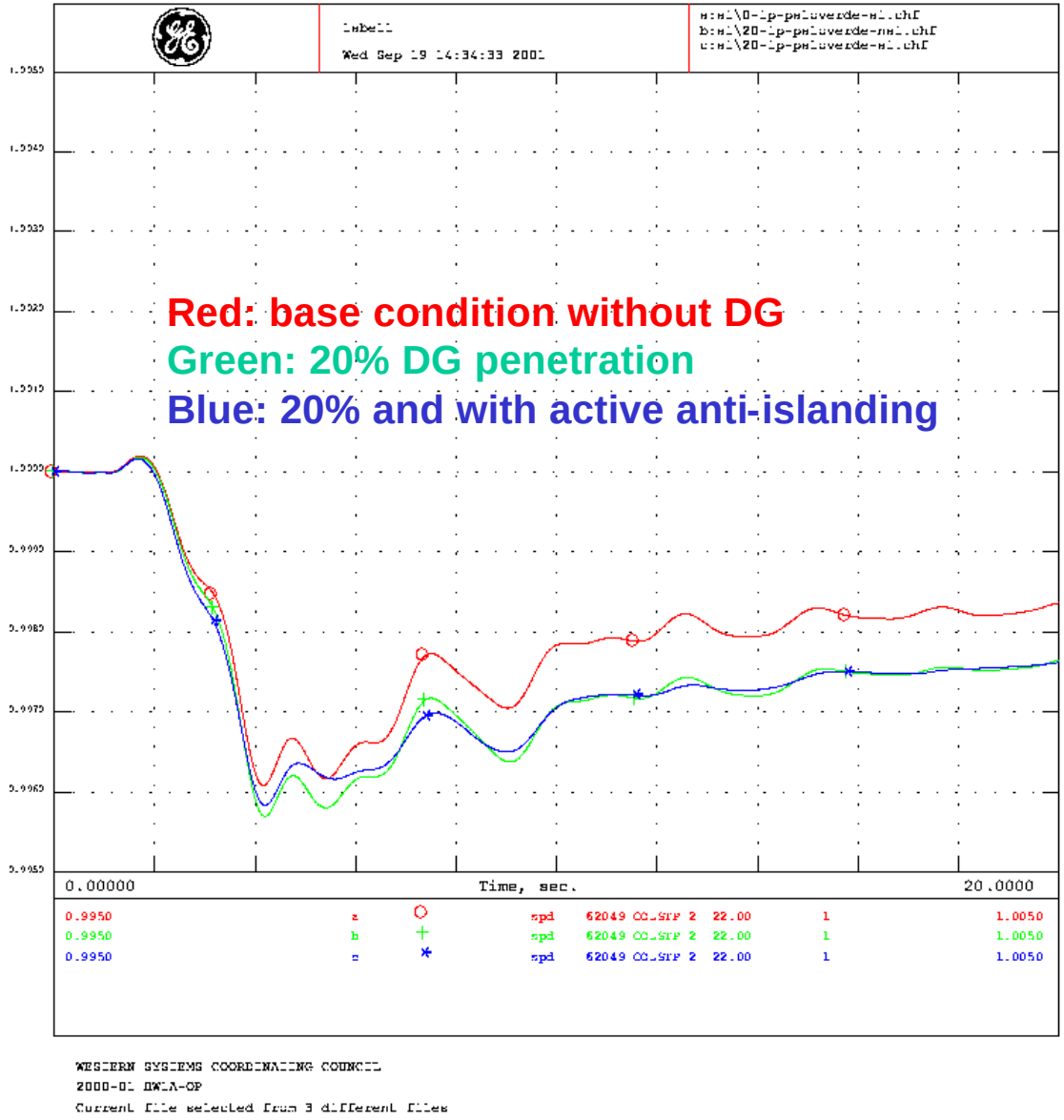

Adding DG

**DG + Load Bus Representation**




Equivalent Load:
$P_L (1 + DG_{pene}) + jQ_L (1 + DG_{pene})$

# Active Anti-Islanding Impact on Bulk Power System



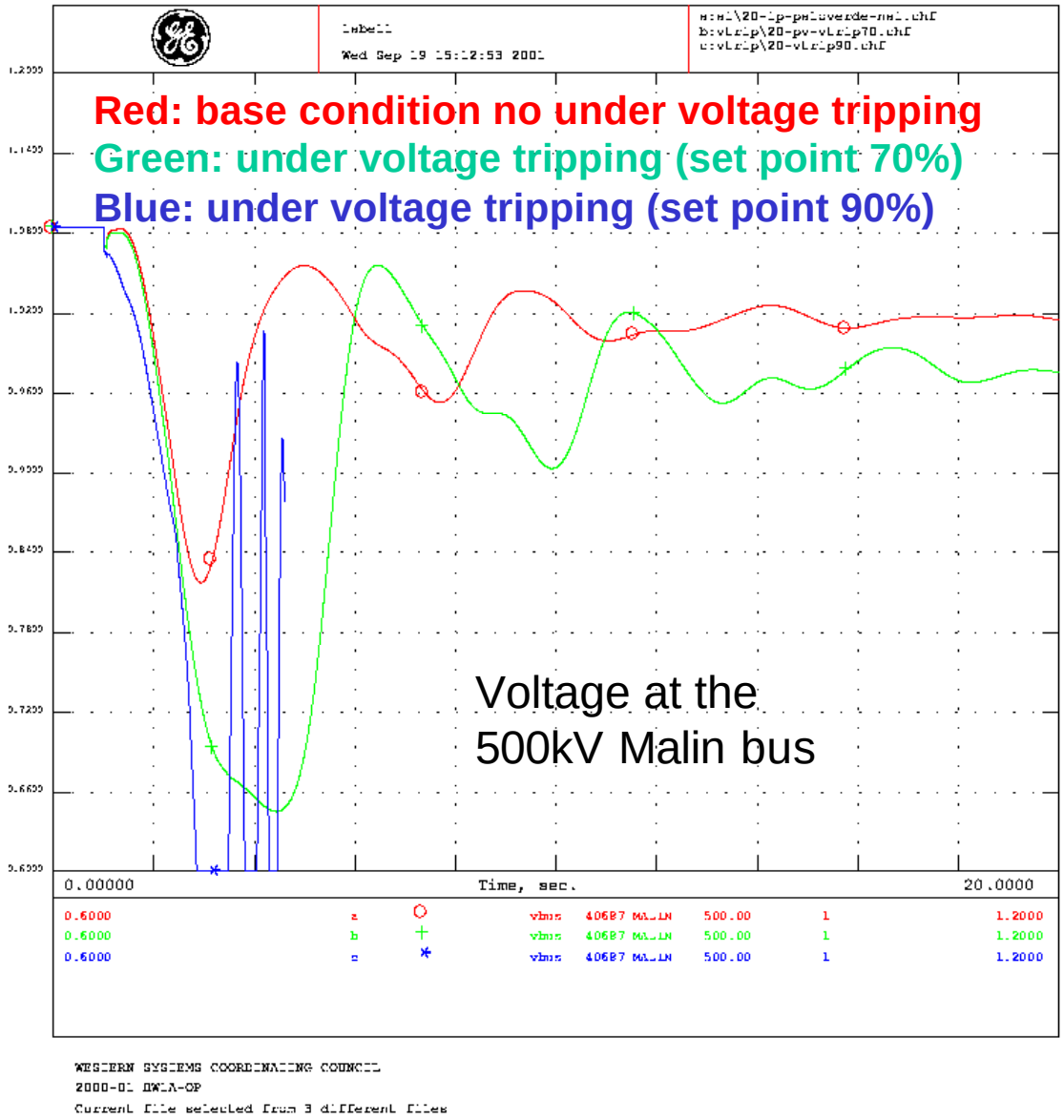

- Disturbance event:
a very large power station with multiple units generating over 3000 MW in WSCC system is assumed to be tripped off-line by some common-mode disturbance.

- The case illustrates that the aggregate impact of the active anti-islanding scheme is benign to the system performance

- The lack of frequency regulation by DGs aggravates the common-mode frequency depression

**Bulk System frequency dynamics with high DG Penetration and impact of Anti-islanding**

# DG Tripping impact on Bulk System Stability




- Most new DGs standards dictate disconnect for voltages <70% for a specified period.

- It is important to note that these documents specify the *minimum* voltage and the *maximum* time to trip. Thus, DGs will be in violation if they trip slower or at too low a voltage. However, the DGs may trip faster and at higher voltages than this without violation.

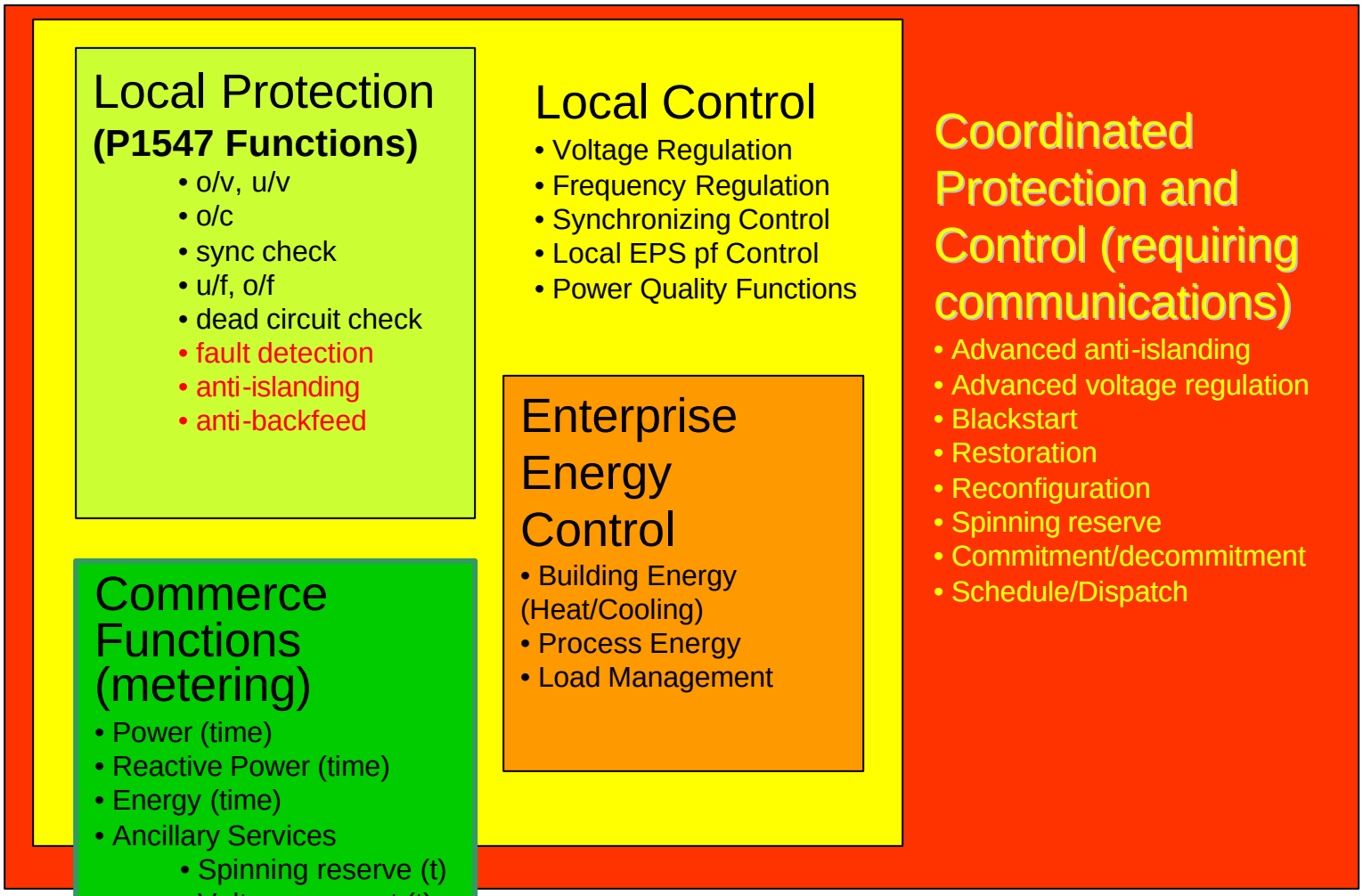
- The case (blue trace) with the 90% trip point is very unstable

Bulk system voltage dynamics with low voltage DG tripping (20% DG penetration).

# Conceptual Interconnect Design

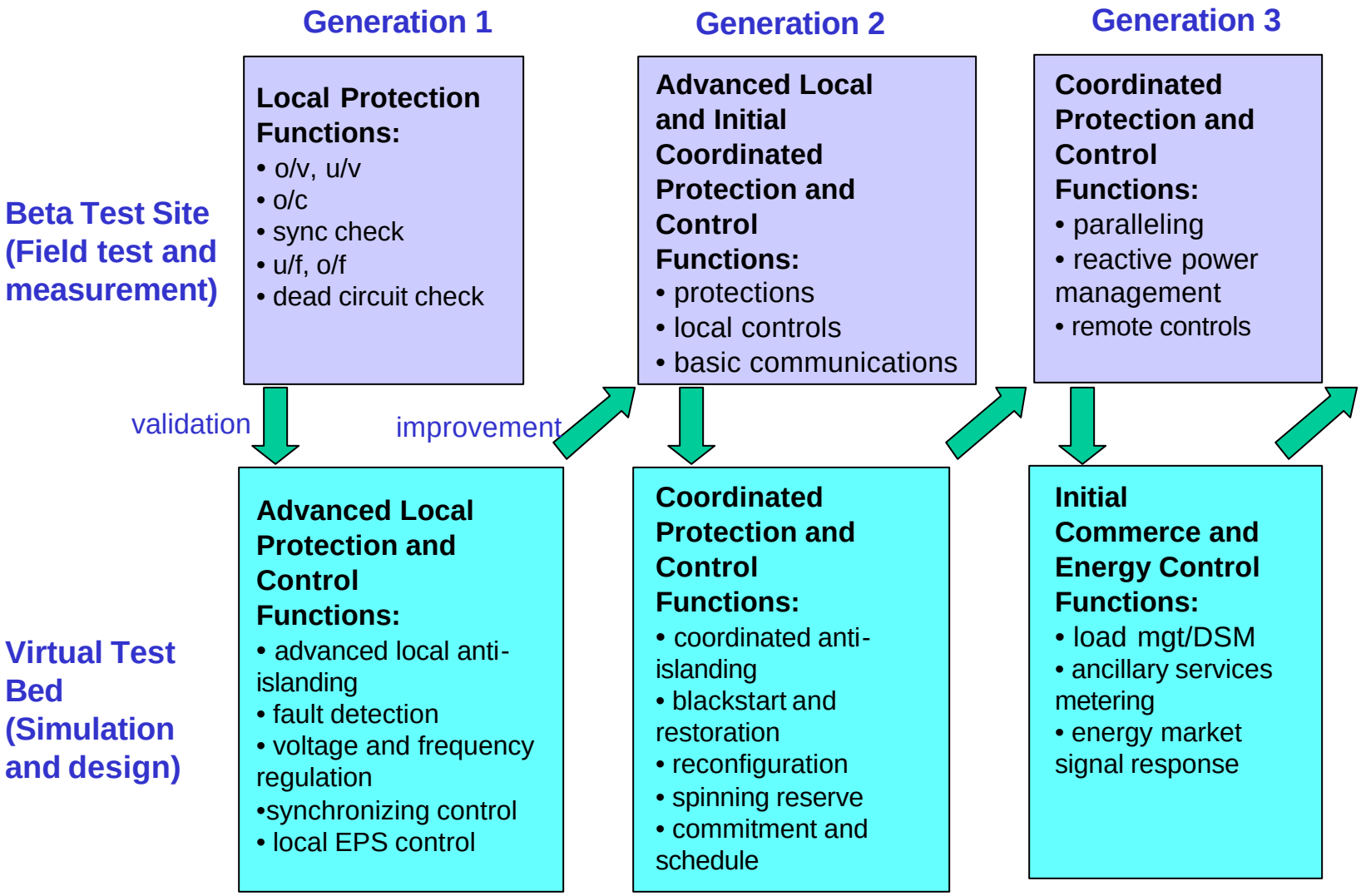
- **Interconnect Needs and Trends**
- **Interconnect Technology Roadmap**
- **Conceived Universal Interconnect Platform**

# Interconnect Needs and Trends



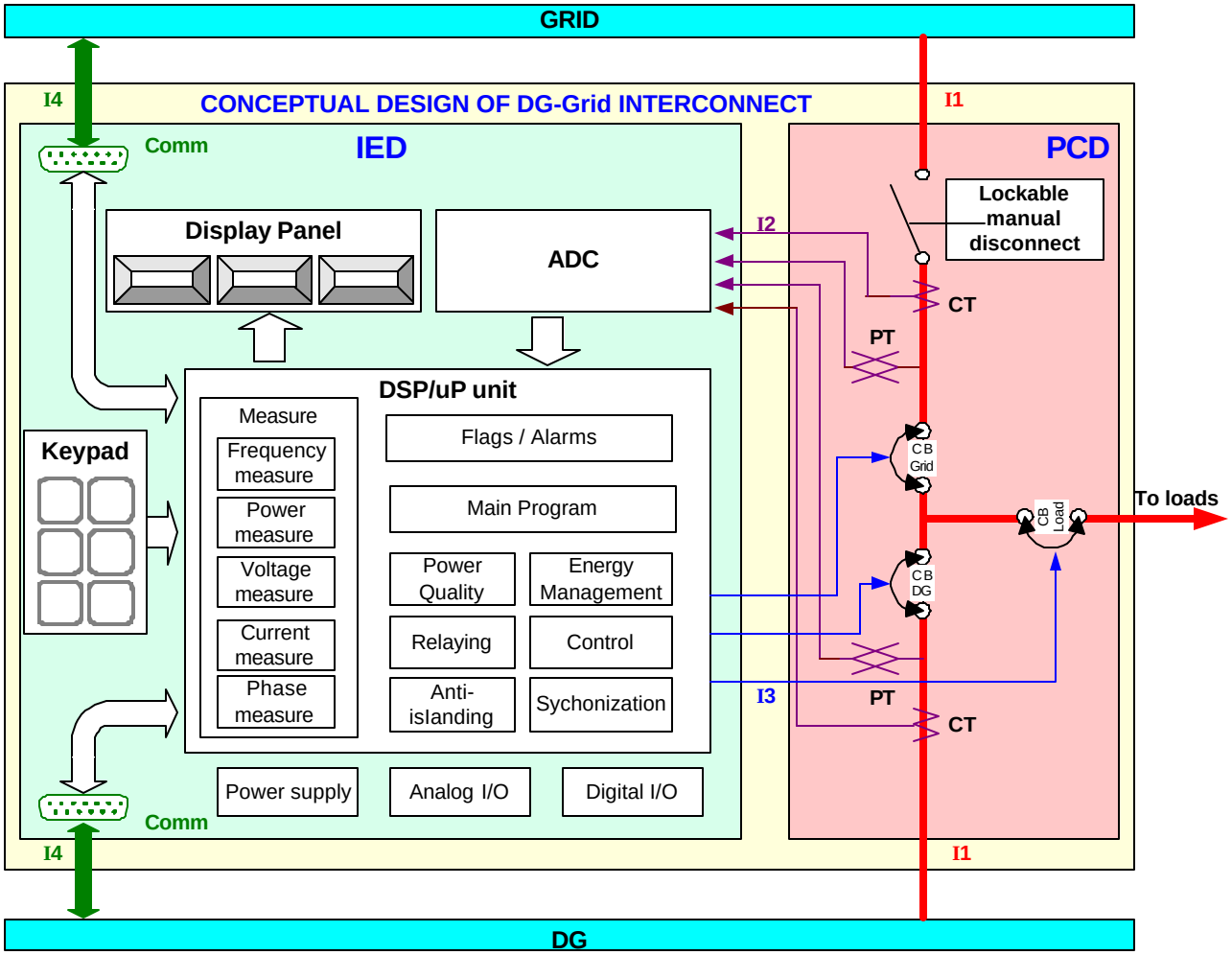

- There is a natural progression of functionality
- Requirements expand at higher penetrations
- Economic benefits increase with higher functionality

# Interconnect Technology Roadmap




• Two vehicles to drive the interconnect technology: Beta Test Site (BTS) for the interconnect prototyping and testing; Virtual Test Bed (VTB) for design, analysis and case studies. The two vehicles interact and support each other.

# Conceptual Interconnect Design




Key Features:

- Standardized modules and interfaces
  - IED
  - PCD
  - Power, comm, sensor and control interfaces
- Technology neutral, suitable for FC, uTurbine, Getset, etc.
- Pre-testing and pre-certification for P1547 compliance
- Scalable and upgradable
- Universal platform with natural progression of functionality
- Ability to maximize the economic and performance benefits of DG

# Future Plan

- Further Case Studies
  - DG high penetration impact
  - Advanced anti-islanding
  - Microgrid
- Prototyping and testing a universal, P1547 compliant Interconnect
- Working with GE business to develop the Universal Interconnect
- Continuing support to P1547

# Technology Transfer and Outreach

- Special presentation to IEEE DG Integration working group meeting at PES Winter Meeting, Jan. 29, 2002
- Organized and chaired DG Panel Session at IEEE T&D Conference, October 2001
- Presentation at IEEE T&D Conference DG Panel Session, October 2001
- Special presentation in IEEE PES Summer Meeting to DG Modeling working group, July, 2001
- 2 invention disclosures filed.

# Summary

- **GE interconnect project is performing crucial investigation of DG and EPS integration issues (Support DPP system integration goal)**
  - Quantitative insight into the critical issues
  - Results are useful to the industry in defining interconnection standards

- **GE proposed a systematic approach to addressing interconnect solutions (Support DPP Interconnection cost reduction goal)**
  - Reduce hassle factor in the interconnection process through pre-testing and pre-certification of standard-compliant interconnects.
  - Achieve full benefits and value for DG through a universal interconnect platform with modular, scalable and progressive functionalities.

- **The "surface has been scratched"**
  - Fertile ground for further investigation

**Making the correct choices now provides for the future of DG**